



**Cihan University**  
**College of Science**  
**Department of Computer**

## **Course Book**

### **CSC1203 parallel processing**

**Year:** 4<sup>th</sup> / *Computer Department*

**Semester:** 2<sup>nd</sup>

**Academic Year:** 2014 / 2015

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**Class Time:** 1-hour, *Wednesday (12:30 PM -1:30 PM)*

*: 1-hour, Thursday (10:30 PM- 11:30 PM) .*

#### **Assessment Method**

Mid Semester Exam	30%
Quizzes & Assignments	5%
Attendance, H.W. and Activity	5%
Final Semester Exam	60%

#### **List of Recommended Text Books**

<b>1-</b> F. B. Moreshwer, <b>Parallel Computing</b> , Addison-Wesley Publishing Company, 2008.
<b>2-</b> M. Morris Mano, <b>Computer System Architecture</b> ,3 <sup>rd</sup> edition.
<b>3-</b> Hesham El-Rewini, Mostafa Abd-El-Barr, <b>Advanced Computer Architecture And Parallel Processing</b> , Wiley, 2005.
<b>4-</b> David A. Patterson, Hohn L. Hinnessy, <b>Computer Organization and design: the hardware / Software interface</b> . 3 <sup>rd</sup> edition, Elsevier, 2005.

## **Syllabus**

### **1. Introduction:**

- 1.1- Basic Computer.
- 1.2- Parallel Computing.
- 1.3- Applications & Importance.
- 1.4- Some General Parallel Terminology.

### **2. Architecture Classifications:**

- 2.1- Flynn's Classification.
- 2.2- Shore's Classification.
- 2.3- Feng's Classification.
- 2.4- Handler's Classification.

### **3. Parallel Computing Architecture:**

- 3.1- Introduction.
- 3.2- Parallelism types.
- 3.3- Multiprocessors.
  - 3.2.1-Synchronous Multiprocessors(Array processors).
  - 3.2.2- Asynchronous (Conventional) Multiprocessors.
- 3.4- Memory architectures:
  - 3.4.1- Shared Memory (Tightly Coupled).
    - A- Uniform Memory Access (UMA).
    - B- Non-uniform Memory Access (NUMA).
  - 3.4.2- Distributed Memory (Loosely Coupled).
    - A-Grid.
    - B-Cluster.
  - 3.4.3- Hybride Shared and Distributed Memory.

### **4. Performance of Parallel Processing:**

- 4.1- Speedup & Efficiency.
- 4.2- Amdahl's Law.

4.3- Minsky's Conjecture.

4.4- Gustafson's Law.

## **5. Pipeline Processing:**

5.1- Pipeline Definition.

5.2- Pipeline Performance in terms of Parallel Processing.

5.3- Arithmetic Pipeline.

- Floating Point Adder-Subtractor Architecture.

- Floating Point Adder-Subtractor Performance.

5.4- Instruction Pipeline.

- RISC Instruction Architecture.

- RICS Instruction Performance.

## **6. Interconnection Network and Classification.**

6.1- Direct Connection Networks

6.2- Indirect Connection Networks .

6.2.1- Busses .

6.2.2- Multistage networks.

6.2.3- Crossbar switches.

## **7. Load Balancing.**

- Three or four Quizzes.
- 2 or 3 Assignments.